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Nabil Shovon Ashraf

Parameter-Centric Scaled FET Devices

Physics Based Perspectives and Attributes

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Preface

This book authored by Dr. Nabil Shovon Ashraf and entitled *Parameter-Centric Scaled FET Devices* chronologically discusses in the Introduction section and Chaps. 1–8, the material and device transport parameters that are critical for FET devices at advanced node architectures such as gate all around (GAA) nanowire FET and vertically stacked GAA nanosheet FET. Most of the previous modeling of some of these parameters that define FET drive current, mobility and saturated drift velocity from T = 300 K to cryogenic temperature exclude band nonparabolicity effect on conduction band minima and valence band maxima due to high degenerate doping for silicon. This book extracts parameters such as activated dopant percentage that generates free carrier concentration, density of states effective mass for electron and hole for silicon and conductivity effective mass for electron and hole for nondegenerate doping concentrations for cryogenic temperatures up to 50 K which are done through precise analytical equations from T = 4.2 K experimental data for silicon. Since band nonparabolicity is a function of temperature distinctively for each particular doping concentration between $10^{17}/cm^3$ to $10^{21}/cm^3$, their derivation in analytical form requires a huge set of data from measurements or modeling at T = 300 K for silicon which has not been done so far.

Industry TCADs like Silvaco and Synopsys Quantum ATK tool report the density of states' effective mass of electron and hole values for silicon at T = 300 K with imprecise substitutions for simulation purposes. This book correctly quotes these values along with conductivity effective mass values both for nondegenerate doping of silicon substrate and non-linear incremental approach-based effect of band nonparabolicity on these two types of effective masses in silicon at T = 300 K for degenerate doping concentrations. 3D band structure-based density functional theorem (DFT) and full band 3D quantum simulation methods might generate FET transport values such as drive current, subthreshold leakage current, threshold voltage, Ion/Ioff inversion channel mobility and saturated drift velocity under ballistic transport but does not intrinsically report the density of states effective mass values or conductivity effective mass values of majority or minority carrier FETs in a precise way. The parameters generated in this book from Chaps. 1–5 can be

used in TCAD simulators and other device transport analysis-based simulators like DFT, full band 3D quantum simulation and Ensemble Monte Carlo simulation techniques and benchmark parameters then will be more precisely defined as these parameters have analytical equations based on computability as narrated in Chaps. 1–5. Material properties are key for all materials where these FET devices are fabricated other than silicon material and mostly their ballistic transport efficiency is pivotal like silicon substrate in cryogenic temperatures where certain device physical analyses of these parameters become critical and are discussed in final Chap. 8. This book will enlighten and deepen the learning of device physics and engineering professionals who work on FET architectures based on device fabrication, modeling and reliability assessments at advanced nodes.

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Introduction

Why the author of this book notes that there are critical modeling requirements that have not been properly discussed todate by various illustrious textbooks [1–4]. Before reference [6] first showed that the general accepted theory that incomplete ionization of dopants in n-type and p-type silicon only existed as low temperatures of operation such as T = 100 K to below down to cryogenic temperature T = 4.2 K and also attributed improperly that for degenerate doping above than $10^{19}/cm^3$ substrate doping in silicon for both p-type and n-type doping in silicon, incomplete ionization plays a role. Reference [6] proves these established theories wrong that generally in n-type silicon with phosphorous doping and p-type silicon with boron doping, the incomplete ionization at T = 300 K stays close to 100% between $10^{15}/cm^3$ and $10^{17}/cm^3$ and then the ionization gradually drops to almost 80% for n-type phosphorous doped silicon and near 70% for p-type boron doped silicon between $10^{17}/cm^3$ and close to $10^{19}/cm^3$. From $10^{19}/cm^3$, the ionization starts to increase quickly and reaches full 100% for $10^{21}/cm^3$–$10^{22}/cm^3$ for both n-type phosphorous and p-type boron doped silicon at T = 300 K excluding dopant values close to silicon maximum dupability limit ($5 \times 10^{22}/cm^3$). So we can see that, the general accepted theory that low temperature operation generates incompletely ionized free carriers are acceptable but degenerate doping levels between few $10^{18}/cm^3$ to $10^{21}/cm^3$ generate incomplete ionization in silicon is wrong, rather the incomplete ionization that is experimentally demonstrated in [6] is actually in the non-degenerate doping levels ($10^{17}/cm^3$–few $10^{18}/cm^3$) and slightly degenerate doping levels (few $10^{18}/cm^3$–$10^{19}/cm^3$) and for general high degenerate doping level in silicon for p-type and n-type at T = 300 K, there is actually complete ionization at T = 300 K.

This observation of reported incomplete ionization modeling in [6] provides us a completely novel step by step analytical equation-based approach where before using Fermi-Dirac integral, first we need to know ionized free carrier density in silicon for n-type and p-type silicon at T = 300 K taking the Phosphorous and Boron as dopants and compute this carrier density (ionized) from provided substrate doping data or information. Correctly knowing this completely ionized free carrier density at a particular

substrate doping density assuming neutral also gives us reassessment of the curve where free carrier density reduction due to complete ionization computation, changes the associated Fermi-Dirac integral value from the curve shown in [1] and the corresponding integral parameter eta_c = (E_f-Ec)/kT and eta_v = (E_v–E_f)/kT shown in [1]. The steps are now (1) first to determine ionized free carrier density in n-type and p-type silicon at T = 300 K taking a substrate doping [6], (2) calculate the Fermi-Dirac integral from [1] and integral parameter eta_c and eta_v from [1]. (3) Then we can verify how accurate the Fermi-Dirac integral value based on ionized free carrier computation by taking equations in [5] where knowing eta_c and eta_v corresponding Fermi-Dirac integral can be numerically calculated, and the error percentage generally remains within 0.5% for all doping levels mainly non-degenerate to degenerate transition zone (10^{17}/cm^3 and above) and for degenerate zone (10^{18}/cm^3 to 10^{21}/cm^3).

Band nonparabolicity of density of states (DOS) effective masses for electron and hole in silicon at T = 300 K at degenerate doping levels for the values mentioned above in silicon are also not accurately reported except reference [4]. Reference [4] reports the DOS effective masses for degenerate doping levels in silicon for electron for T = 300 K and other temperatures where effective mass increase of silicon for T = 300 K for electron in the DOS case, is seen to rise above than 1.6 times than room temperature nondegenerate effective mass in silicon for electron, i.e., 1.18 m_o where m_o is free electron mass. The author also witnesses wrongly reported DOS effective mass values at T = 300 K for silicon for electron and hole. Only [1], [2] and [4] report the DOS effective mass values at T = 300 K for silicon for the case of electron and hole to be 1.18 m_o and 0.81 m_o, which is very crucial in determining many parameters for field effect transistors (FET), for instance, effective density of states in the conduction and valence band in silicon for T = 300 K which determine inversion carrier density in FET as a function of gate voltage, intrinsic carrier concentration at T = 300 K for silicon for non-degenerate doping values [11–13] taking the correctly quoted masses from [1], [2] and [4] which may not have been correctly quoted in [11–13]. Conductivity effective masses for silicon at T = 300 K for electron and hole are not also fully correctly reported by any of these textbook references [1–4]. So, the author of this book first calculated the conductivity effective masses for electron and hole in silicon for T = 300 K for non-degenerate doping levels taking analytically solvable equations from [4] and also [3]. Conductivity effective masses also need precise calculation as these determine the drift mobility of channel carriers in n-type and p-type FETs where the gate voltage and drain voltage also play role by introducing carrier scattering. So, from well-known reported mobility-doping concentration figures for majority carriers and minority inversion carriers such as [17], using Drude equation and knowing conductivity effective masses of electron and hole in silicon at T = 300 K at a specific substrate doping taking non-degenerate doping into consideration, total scattering time can be determined for low drift field. Now, band nonparabolicity also affects the conductivity effective masses of electron and hole in silicon at T = 300 K when the doping degenerates and this will modify the mobility and scattering times seen

in [17] for high degenerate substrate doping where the actual mobility reduction factor is not ionized impurity scattering but surface roughness scattering but [17] only reports ionized impurity scattering-related mobility values as a function of substrate doping up to degenerate level and information about subthreshold mobility, ionized impurity scattering, thermally limited phonon scattering-related mobility peak value, transition to optical phonon scattering and surface roughness scattering can be seen from plots in [18] as a function of vertical electric field in n-MOSFET with low lateral field or drain voltage. Here also incomplete ionization modifies the ionized carriers and the screening of dopants for subthreshold mobility and surface roughness scattering, the latter should be more intense for degenerate substrate doping values in n-FET where the carriers are 100% ionized. Furthermore, [18] is inaccurate for inversion layer mobility in the doping range 10^{17}/cm^3 to 10^{19}/cm^3, where [18] generally assumed complete ionization for non-degenerate doping levels where values such as 10^{17}/cm^3 to few 10^{18}/cm^3 lie. Since, [6] shows that there is incomplete ionization of dopants in silicon at T = 300 K for both n-type phosphorous and p-type boron between 10^{17}/cm^3 to 10^{19}/cm^3 dopant values, therefore for gate bias in subthreshold region, there will be neutral impurity scattering to be considered for inversion layer mobility in [18] which reports data for T = 300 K and T = 77 K. For neutral impurity scattering, for n-MOSFET, inversion electrons face less repulsive field than negatively ionized acceptors in the depletion region, as a result, neutral impurity scattering increases subthreshold mobility and inversion layer mobility for both linear and saturation region when gate overdrive is low or the phonon-related mobility peak has not been reached. The author of this book recalculated the conductivity effective masses for electron and hole in silicon for T = 300 K from nondegenerate to degenerate substrate doping levels taking a ratio-based increase of masses due to band nonparabolicity. Analytical equations for DOS and conductivity effective masses for electron and hole in silicon at T = 300 K up to degenerate substrate doping were very much important from FET transport parameter calculations such as inversion charge density, drift mobility, saturated drift velocity at T = 300 K that determine the FET drive current and that was the sole purpose of this book that staring from accurate completely ionized dopant information, from Fermi-Dirac integral value and then corresponding eta_c and eta_v values, bulk Fermi level energy Ef can be determined, band gap narrowing from ionized dopant-related conduction band minima peak decrease and valence band maxima increase taking equations from [10] and hence the bulk potential for threshold voltage determination generally for degenerate doping substrate dopant values. Intrinsic Fermi energy level Efi for degenerate doping case can be determined from correctly computed intrinsic carrier concentration taking the references [6] and [10] and that exactly the author focused upon as the bulk potential can be known by knowing the intrinsic Fermi energy Efi and actual Fermi energy Ef.

Next the references as we go along [14–16] all need revision as per correctly computed ionized dopants from [6], changes in Fermi-Dirac integral and integral parameters

eta_c and eta_v, band nonparabolicity induced density of states, effective masses for electron and hole now need to be calculated as a function of temperature and doping up to degenerate doping levels both, ionized dopant-related changes in band gap narrowing parameter as scripted [10] and making it function of temperature. Reference [19] reports the proper application rule of Matthiesen's equation to combine various scattering events in n and p-type silicon substrates and FETs. References [20–22] are very important references for scaled FET architecture overview and how 2D scaling length parameter optimizes the short channel effect (SCE) in FET but all calculations must proceed from defining ionized dopant data first and then converting it to free carriers. Fermi-Dirac integral should be used in these references [20–22], although the substrate doping in the nondegenerate regime indicates that Maxwell-Boltzmann equation use would not alter percentage error above 0.5% for all the parametric modeling data reported in these references [20–22]. Reference [23] is an important reference for scaling theory to be applied to control short channel effects (SCE) for fully depleted cylindrical and surrounding gate MOSFETs, which will be useful in studying stacked nanosheet gate all around MOSFETs, where currently FinFET like fin type gate structure is fabricated. For thin silicon film, if fully depleted cylindrical and surrounding gate structure like gate all around GAA FET can be employed for nanosheet n-FET, using scaling theory, it can be determined how volume inversion for low gate voltage can be achieved in this nanosheet FET. Volume inversion of carriers reduces boundary layer scattering and surface scattering induced self-heating effect (SHE) that is conspicuously observed in this type of considerable fin-height and width-based gate stack.

References [24–27] focus upon gate tunneling leakage current optimization which increases at a higher rate than subthreshold leakage current as the FET nodes are scaled. Modeling and computation of these gate tunneling leakage current being also necessary for nearly 1–2 nm effective oxide thickness including high-k oxides and reduction of gate tunneling leakage current from optimizing device parameters of FET are mentioned in [24–26]. Reference [27] shows that 2D material such as MoS_2 is capable of showing much lower tunneling leakage current than silicon. The lowest interface defect density requires a seamless oxide-semiconductor interface and for that process such as atomic layer deposition (ALD) is mandatory and references [28] and [29] discuss this. References [30–35] discuss scaling effects on nanoscale MOSFET from performance benchmarking. Reference [36] is an important inclusion in this book that shows through Ensemble Monte Carlo simulation, the thermal effects of nanoscale MOSFETs, where the channel carrier temperatures can rise many kelvin over than room temperature $T = 300$ K setting the transport to be at non-equilibrium, and this paper also shows that heating effects get pronounced near drain before thermalization and therefore, in saturation region where the drain voltage is higher, the inversion layer carriers may undergo thermal heating effects. Boundary layer scattering and surface roughness scattering in thin silicon film such as FinFET, gate all around (GAA) nanowire FET and fully depleted silicon on insulator (FD-SOI) FET suffer additionally from self-heating effects where the temperatures of the

channel carriers remain higher than substrate temperature during on-current condition as silicon's thermal conductivity is lower and cannot dissipate the heat faster than material such as SiO_2 and diamond. In FD-SOI case, self-heating effect is minimized for thin silicon buried-oxide (BOX), which has higher thermal conductivity than the silicon film that is fully depleted and generally more thinned than BOX. Thin BOX of FD-SOI also enables BOX-film interface to be having a sheet of positive potential by applying negative voltage on the back gate, so the inversion layer electrons are slightly pulled away in the silicon film by the attractive force of the BOX-silicon back gate interface sheet positive charge and inversion carriers. This reduces boundary layer scattering at the front gate oxide-silicon film interface and also surface roughness scattering for FD-SOI and hence self-heating effects (SHE).

Reference [37] is a rigorous analysis of quantum transport in field effect transistors, importantly for scaled nodes around 10 nm. References [38–42] discuss the cryogenic temperature device physics and operational characteristics of FETs. References [43–46] are based on multigate architecture all the way to gate all around (GAA) nanowire FET, which is the norm for present FET architecture due to improved gate to channel integrity, uniform channel thickness and operation region in the low nondegenerate substrate doping allowing volume inversion of channel carriers as the GAA nanowire pore dimension gate smaller. Self-heating effects (SHE) that degrade threshold voltage and FET transconductance for GAA FET with cylindrical and fin-type gates and also for reduced pore diameter are also discussed in couple of these references [43–46, 53–54]. References [47–52, 55] discuss the most recent FET architecture progressing from GAA to nanosheet with vertical gate stack and also complementary FET or C-FET form. Some of these critically important reference articles are further analyzed in various chapters of this book by the author of this book. Some factual contents regarding advanced node FETs are arbitrary and do not require particular reference citation to be indexed.

The author of this book has arranged the chapters as follows. Chapter 1 discusses all the parametric computation related to incomplete ionization in silicon at T = 300 K for the doping levels between $10^{17}/cm^3$ to few $10^{19}/cm^3$. Band nonparabolicity that changes DOS effective masses for electron and hole in silicon and associated change in incomplete ionization or ionized dopant data are also calculated and plotted with different perspectives of illustration in Chap. 2. Chapter 3 discusses the DOS and conductivity effective masses of electron and hole in silicon at T = 300 K between $10^{17}/cm^3$ and $10^{19}/cm^3$ with nondegenerate to degenerate regime and with ratioed increase of band nonparabolicity for different ranges of degenerate substrate doping. For non-degenerate substrate doping, based on full ionized dopants (doping in the range $10^{16}/cm^3$), DOS and conductivity effective masses of electron and hole as a function of substrate temperature down to 4.2 K can be determined by three-term polynomial method but these equations are not derived in Chap. 3 as band nonparabolicity effect is temperature dependent for a particular doping concentration. Analytical equation format DOS and conductivity effective masses for electron and hole in silicon derivation are complicated for higher nondegenerate to degenerate doping

levels where band nonparabolicity itself becomes function of temperature distinctively for each dopant. So that calculation is omitted. Also discussed are scattering time extraction using Drude mobility model and extracted conductivity effective masses of electron and hole with band nonparabolicity for degenerate doping.

Chapter 4 discusses the Drude mobility for majority and minority carriers of electron and hole in FETs, effective intrinsic carrier concentration (n_{ieff}) for silicon at T = 300 K taking ionized dopant into consideration and ionized dopant induced band gap narrowing into consideration and now this n_{ieff} is shown to be different for n-type and p-type substrate and generally has a increasing trend between $10^{17}/cm^3$ to few $10^{19}/cm^3$. DOS masses for electron and hole for majority n-type and majority p-type silicon at T = 300 K are recalculated in the presence of band nonparabolicity to calculate overall n_{ieff}, other parameters like Fermi level E_F, band gap E_G, bulk potential φ_B and substrate resistivity ρ are also calculated taking the effect of band nonparabolicity on degenerate substrate doping for both n-type and p-type silicon at T = 300 K. Chapter 5 discusses the advantages of operating FET devices in cryogenic temperatures and some of the bottlenecks that need to be overcome for ensuring higher drive current than T = 300 K operation. Neutral impurity scattering which is present in silicon at T = 300 K for certain incompletely ionized nondegenerate doping values and also for temperatures as low as cryogenic temperatures is discussed in a sub-section of this Chap. 5. Chapter 6 discusses the current progress on GAA nanowire FET performance improvement. Chapter 7 discusses the stacked vertical nanosheet FET and one of the focus of this chapter is the self-heating effects in GAA and nanosheet FET and its minimization strategy and issues arising from random discrete channel dopants out of confinement by gate stack. Chapter 8 elucidates the conclusion on understanding of Chaps. 1–7, future directions and insights on the modeling requirement of parameters to be analytically computable for FET devices fabricated in material other than silicon at T = 300 K down to cryogenic temperature level operation. List of references is finally appended to this book.

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